19-5001; Rev 1; 5/10

EVALUATION KIT AVAILABLE

3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

General Description

The MAX2842 single-chip, direct-conversion, zero-IF RF transceiver IC is designed for 3GHz NLOS wireless broadband MIMO systems. It has two transmitters and two receivers, with differential 100Ω RF inputs and outputs. The IC includes all circuitry required to implement the complete RF transceiver function, providing fully integrated receive paths, transmit path, VCO and tank, frequency synthesis, and baseband/control interface. It includes a fast-settling sigma-delta RF fractional synthesizer with ~25Hz frequency step size. The IC also integrates an on-chip AM detector for measuring transmitter I/Q imbalance and LO leakage. An internal transmit-to-receive loopback mode allows for receiver I/Q imbalance calibration. The IC supports full duplex mode of operation for external loopback.

The MAX2842 completely eliminates the need for external SAW filters by implementing on-chip programmable monolithic filters for both receiver and transmitter, for channel bandwidths from 3.5MHz to 10MHz. The baseband filtering Rx and Tx signal paths are optimized to meet stringent noise figure and linearity requirements. The transceiver is housed in a small 56-pin TQFN, 7mm x 7mm, leadless plastic package with exposed paddle.

Applications

3GHz 16d and 16e MIMO WiMAX

Features

- **3.3GHz to 3.9GHz Operation**
- **Complete RF Transceiver with PA Driver**
  - **0dBm Linear OFDMA Transmit Power, 64-QAM, -65dB Relative Spectral Emission Mask**
  - **3.8dB Receiver Noise Figure**
  - **Automatic On-Chip Receiver I/Q DC Cancellation**
  - **On-Chip Tx I/Q Gain/Phase Error and LO Leakage Detection**
  - **Monolithic Low-Noise VCO with -38dBc Integrated Phase Noise**
  - **Fully Integrated Programmable I/Q Lowpass Rx Channel Filters for 3.5MHz, 5MHz, 7MHz, and 10MHz Channels**
  - **Programmable Tx I/Q Lowpass Reconstruction Filters**
  - **Fractional PLL with 50µs Channel Hopping Time (Settling to 50Hz)**
  - **4-Wire Bidirectional SPI™ Interface**
  - **60dB Transmit Power Control Range, Digitally Controlled by SPI**
  - **71dB Receive Gain Control Range, Digitally Controlled by SPI**
  - **RSSI with 60dB Dynamic Range**
  - **Digital Control for Tx, Rx, Shutdown, and Standby Modes**
  - **On-Chip Crystal Oscillator with Digital Tuning**
  - **Programable Logic Interface Voltages**
  - **Both Automatic and Modem-Assisted Receiver I/Q DC Offset Correction**
- **Single +2.7V to +3.6V Supply**
- **Low Shutdown Mode Current**
- **Small 56-Pin TQFN Package (7mm x 7mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2842ETN+T	-40°C to +85°C	56 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Typical Operating Circuit appears at end of data sheet.

SPI is a trademark of Motorola, Inc.

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ Pins to GND .....-0.3V to +3.9V
RF Inputs: Maximum Current at RXINA+, RXINA-, RXINB+, RXINB- ..... -1mA to +1mA
RF Outputs: TXOUTA+, TXOUTA-, TXOUTB+, TXOUTB- to GND.....-0.3V to +3.9V
Analog Inputs: TXBBIA+, TXBBIA-, TXBBQA+, TXBBQA-, TXBBIB+, TXBBIB-, TXBBQB+, TXBBQB-, REF_DIG to GND .....-0.3V to +3.9V
Analog Input: XTAL1, REF_OSC .....AC-Coupled Only
Analog Outputs: Maximum Current at RXBBIA+, RXBBIA-, RXBBQA+, RXBBQA-, RXBBIB+, RXBBIB-, RXBBQB+, RXBBQB-, CPOUT+, CPOUT- ..... -1mA to +1mA
Analog Outputs: Maximum Current at PABIAS_A, PABIAS_B..... -100mA to +100mA
Digital Inputs: TXRX, $\overline{CS}$, SCLK, DIN, ENABLE, CLKOUTEN to GND.....-0.3V to +3.9V
Digital Outputs: DOUT, CLKOUT.....-0.3V to +3.9V
Bias Voltages: BYP_VCO .....-0.3V to +3.9V
Short-Circuit Duration on All Output Pins..... 10s
RF Input Power: All RXIN_..... +10dBm
RF Output Differential Load VSWR: All TXOUT_..... 6:1
Continuous Power Dissipation (T_A = +85°C)
56-Pin TQFN (derate 27.8mW/°C above +70°C) .....< 2222mW
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+260°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS TABLE

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. ENABLE and TXRX are set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 90mV_{RMS} differential I and Q signals (1MHz) applied to I and Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 3.6GHz, and T_A = +25°C, unless otherwise noted. LOGIC_VREF = $V_{CC\_}$.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage, V_{CC}			2.7		3.6	V
Supply Current	Shutdown mode			10		µA
	Shutdown mode with 44.8MHz reference clock output			1.9	3.6	mA
	Shutdown mode with crystal oscillator enabled and 44.8MHz reference clock output			2.9	5.0	
	Standby mode			35	50	
	Rx mode	One receiver on		77	96	
		Both receivers on		115	142	
	Tx mode	One transmitter on		152	190	
		Both transmitters on		246	320	
	Receiver loopback I/Q calibration	One receiver on		125	155	
		Both receivers on		154	190	
	Transmitter calibration with AM detector	One transmitter on		119	148	
		Both transmitters on		181	230	
Rx I/Q Output Common-Mode Voltage	D5:D4 = 00 in Local address 8			1.0		V
	D5:D4 = 01 in Local address 8		0.77	1.1	1.32	
	D5:D4 = 10 in Local address 8			1.2		
	D5:D4 = 11 in Local address 8			1.3		

DC ELECTRICAL CHARACTERISTICS TABLE (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = -40°C to +85°C, Rx set to the maximum gain. ENABLE and TXRX are set according to operating mode, $\overline{CS}$ = high, SCLK = DIN = low, no input signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 90mV_{RMS} differential I and Q signals (1MHz) applied to I and Q baseband inputs of transmitter in transmit mode, all registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at $V_{CC\_}$ = 2.8V, f_{LO} = 3.6GHz, and T_A = +25°C, unless otherwise noted. LOGIC_VREF = $V_{CC\_}$.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx Baseband Input Common-Mode Voltage Operating Range	To achieve at least +4dBm Tx output P - 1dB with maximum -3dB gain setting	0.5		1.2	V
Tx Baseband Input Bias Current	Source current		10	25	µA
LOGIC INPUTS: TXRX, ENABLE, SCLK, DIN, $\overline{CS}$, CLKOUTEN					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4V			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: DOUT, CLKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4V			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V
DOUT Voltage in Shutdown Mode or Disabled Mode	D7:D5 = 000 in Main address 22		V_{OL}		V
CLKOUT Voltage When Disabled			V_{OL}		V

AC ELECTRICAL CHARACTERISTICS TABLE—Rx Mode

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, baseband output signal frequency = 1MHz, receiver baseband I/Q output at 90mV_{RMS}, REF_OSC frequency = 44.8MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low. Lowpass filter is set to 10MHz RF channel BW, with power matching for the differential RF pins using the *Typical Operating Circuit*. RXBB_ pins are loaded with differential 10kΩ resistor and 10pF capacitance in parallel. Registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SYSTEM: RF INPUT TO I/Q BASEBAND LOADED OUTPUT						
RF Input Frequency Range			3.3		3.9	GHz
Peak-to-Peak Gain Variation Over RF Input Frequency Range	Tested at band edges and band center; at one temperature			3		dB
S11 of RF Input Port	All RF gains			-10		dB
Total Voltage Gain	T_A = -40°C to +85°C	Maximum gain; D7:D0 = 11111000 in Main address 2 for Rx1, in Main address 3 for Rx2	70	77		dB
		Minimum gain; D7:D0 = 00000111 in Main address 2 for Rx1, in Main address 3 for Rx2		6	14	

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AC ELECTRICAL CHARACTERISTICS TABLE—Rx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, baseband output signal frequency = 1MHz, receiver baseband I/Q output at 90mV_{RMS}, REF_OSC frequency = 44.8MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low. Lowpass filter is set to 10MHz RF channel BW, with power matching for the differential RF pins using the *Typical Operating Circuit*. RXBB_ pins are loaded with differential 10kΩ resistor and 10pF capacitance in parallel. Registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RF Gain Steps	From maximum RF gain to maximum RF gain - 8dB (D2:0 = 001 in Main address 2 for Rx1, in Main address 3 for Rx2)		8		dB
	From maximum RF gain to maximum RF gain - 16dB (D2:0 = 010 in Main address 2 for Rx1, in Main address 3 for Rx2)		16		
	From maximum RF gain to maximum RF gain - 24dB (D2:0 = 011 in Main address 2 for Rx1, in Main address 3 for Rx2)		24		
	From maximum RF gain to maximum RF gain - 32dB (D2:0 = 110 in Main address 2 for Rx1, in Main address 3 for Rx2)		32		
	From maximum RF gain to maximum RF gain - 40dB (D2:0 = 111 in Main address 2 for Rx1, in Main address 3 for Rx2)		40		
Gain Change Settling Time	Any RF or baseband gain change; signal amplitude settling to ±0.5dB of steady state, excludes I/Q path DC offset settling		300		ns
	Any RF or baseband gain change; signal amplitude settling to ±0.1dB of steady state, excludes I/Q path DC offset settling		500		
Baseband Gain Range	From maximum baseband gain (D7:D3 = 00000 in Main address 2 for Rx1, in Main address 3 for Rx2) to minimum gain (D7:D3 = 11111 in Main address 2 for Rx1, in Main address 3 for Rx2)	28	31	34	dB
Baseband Gain Step Size			1		dB

AC ELECTRICAL CHARACTERISTICS TABLE—Rx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, baseband output signal frequency = 1MHz, receiver baseband I/Q output at 90mV_{RMS}, REF_OSC frequency = 44.8MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low. Lowpass filter is set to 10MHz RF channel BW, with power matching for the differential RF pins using the *Typical Operating Circuit*. RXBB_ pins are loaded with differential 10kΩ resistor and 10pF capacitance in parallel. Registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DSB Noise Figure	Balun input referred	Voltage gain ≥ 65dB with maximum RF gain (D7:0 = 10111000 in Main address 2 for Rx1, in Main address 3 for Rx2)		3.8		dB
		Voltage gain = 50dB with maximum RF gain - 8dB (D7:0 = 10000001 in Main address 2 for Rx1, in Main address 3 for Rx2)		7.1		
		Voltage gain = 45dB with maximum RF gain - 16dB (D7:0 = 10011010 in Main address 2 for Rx1, in Main address 3 for Rx2)		13.3		
		Voltage gain = 15dB with maximum RF gain - 32dB (D7:0 = 00101110 in Main address 2 for Rx1, in Main address 3 for Rx2)		28.2		
Out-of-Band Input IP3	Two tones at +20MHz and +39MHz offsets, at -35dBm each; measure IM3 at 1MHz	AGC set for -65dBm wanted signal, maximum RF gain (D7:0 = xxxxx000 in Main address 2 for Rx1, in Main address 3 for Rx2)		-15		dBm
		AGC set for -55dBm wanted signal, maximum RF gain - 8dB (D7:0 = xxxxx001 in Main address 2 for Rx1, in Main address 3 for Rx2)		-9		
		AGC set for -40dBm wanted signal, maximum RF gain - 16dB (D7:0 = xxxxx010 in Main address 2 for Rx1, in Main address 3 for Rx2)		-6		
		AGC set for -30dBm wanted signal, maximum RF gain - 32dB (D7:0 = xxxxx110 in Main address 2 for Rx1, in Main address 3 for Rx2)		0		

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AC ELECTRICAL CHARACTERISTICS TABLE—Rx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, baseband output signal frequency = 1MHz, receiver baseband I/Q output at 90mV_{RMS}, REF_OSC frequency = 44.8MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low. Lowpass filter is set to 10MHz RF channel BW, with power matching for the differential RF pins using the *Typical Operating Circuit*. RXBB_ pins are loaded with differential 10kΩ resistor and 10pF capacitance in parallel. Registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Out-of-Band Input IP2	Two tones at +50MHz and +51MHz offsets, at -40dBm each; measure IM2 at 1MHz	AGC set for -65dBm wanted signal, maximum RF gain (D7:0 = xxxxx000 in Main address 2 for Rx1, in Main address 3 for Rx2)		30		dBm
In-Band Input P-1dB	Maximum RF gain (D2:0 = 000 in Main address 2 for Rx1, in Main address 3 for Rx2)			-41		dBm
	Maximum RF gain - 8dB (D2:0 = 001 in Main address 2 for Rx1, in Main address 3 for Rx2)			-32		
	Maximum RF gain - 16dB (D2:0 = 010 in Main address 2 for Rx1, in Main address 3 for Rx2)			-24		
	Maximum RF gain - 32dB (D2:0 = 110 in Main address 2 for Rx1, in Main address 3 for Rx2)			-8		
Output P-1dB Compression	Over passband frequency range, at minimum VGA gain			1.5		V_{P-P}
I/Q Gain Imbalance	1MHz I/Q baseband output, 1σ variation			0.05		dB
I/Q Phase Error	1MHz I/Q baseband output, 1σ variation			0.5		Degrees
Loopback Gain (for Receiver I/Q Calibration)	Transmitter I/Q input to receiver I/Q output; transmitter gain at maximum - 6dB (D5:0 = 000110 in Main address 25), receiver baseband gain = maximum - 10dB (D7:3 = 10101 in Main address 2 for Rx1, in Main address 3 for Rx2) programmed through SPI (Note 2)		2	9	17	dB
I/Q DC Error After Receive Enable	Using one-shot mode, 7µs after receive enable			±15		mV
I/Q Output DC Droop	Averaged both over 10µs, 5µs to 10ms after any gain change or receive enable DC convergence, 1σ variation			±100		µV/ms
Isolation Between Rx Channel A and Rx Channel B				25		dB
RECEIVER BASEBAND FILTERS						
RF Channel BW Supported by BB Filter	Main address 0, serial bits D2:D1 = 00			3.5		MHz
	Main address 0, serial bits D2:D1 = 01			5		
	Main address 0, serial bits D2:D1 = 10			7		
	Main address 0, serial bits D2:D1 = 11			10		
Baseband Gain Ripple	0 to 4.6MHz for BW = 10MHz			1.7		dB_{P-P}
Baseband Group Delay Ripple	0 to 4.6MHz for BW = 10MHz			42		ns_{P-P}

AC ELECTRICAL CHARACTERISTICS TABLE—Rx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, baseband output signal frequency = 1MHz, receiver baseband I/Q output at 90mV_{RMS}, REF_OSC frequency = 44.8MHz, ENABLE = TXRX = $\overline{CS}$ = high, SCLK = DIN = low. Lowpass filter is set to 10MHz RF channel BW, with power matching for the differential RF pins using the *Typical Operating Circuit*. RXBB_ pins are loaded with differential 10kΩ resistor and 10pF capacitance in parallel. Registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications that normally apply over the entire operating conditions, unless otherwise indicated.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Filter Stop Band Rejection	3.5MHz channel bandwidth	1.6MHz		0.5		dB
		2.3MHz		5.5		
		14.25MHz		60		
	5MHz channel bandwidth	2.3MHz		0.5		
		3.3MHz		5.5		
		21MHz		60		
	7MHz channel bandwidth	3.2MHz		0.5		
		4.7MHz		5.5		
		29MHz		60		
	10MHz channel bandwidth	4.6MHz		0.5		
		6.7MHz		5.5		
		41.6MHz		60		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} = 10kΩ			0.5		V
RSSI Maximum Output Voltage	R_{LOAD} = 10kΩ			2.2		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		400		ns
		-32dB signal step		1100		

AC ELECTRICAL CHARACTERISTICS TABLE—Tx Mode

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, ENABLE = $\overline{CS}$ = high, TXRX = SCLK = DIN = low. Power matching at RF outputs using the *Typical Operating Circuit*. Lowpass filter is set to 10MHz RF channel BW; 90mV_{RMS}, 1MHz sine and cosine signal applied to I and Q baseband inputs of transmitter (differential DC-coupled). Registers set to default settings and corresponding test mode, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS					
RF Output Frequency Range		3.3		3.9	GHz
Peak-to-Peak Gain Variation Over RF Band	Single matching for entire band, at one temperature		2.2		dB
Total Voltage Gain	At unbalanced 50Ω matched output		5		dB
Maximum Output Power	OFDMA signal, gain adjusted over maximum gain and maximum gain - 6dB; single matching for entire band; 64-QAM, EVM = -36dB		0		dBm
RF Output Return Loss	All gain settings		6		dB
Output P-1dB	Maximum gain setting		10		dBm

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AC ELECTRICAL CHARACTERISTICS TABLE—Tx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, ENABLE = $\overline{CS}$ = high, TXRX = SCLK = DIN = low. Power matching at RF outputs using the *Typical Operating Circuit*. Lowpass filter is set to 10MHz RF channel BW; 90mV$_{RMS}$, 1MHz sine and cosine signal applied to I and Q baseband inputs of transmitter (differential DC-coupled). Registers set to default settings and corresponding test mode, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Gain Control Range	From maximum Tx gain (D5:D0 = 000000 in Main address 25 for Tx1, in Main address 24 for Tx2) to minimum Tx gain (B6:B1 = 111111)			60		dB
Unwanted Sideband Suppression	Without calibration by modem, and excludes modem I/Q imbalance; sine and cosine signal applied to the I/Q baseband inputs	Maximum Tx gain		45		dB
		Minimum Tx gain		38		
RF Gain Control Binary Weights	D0 in Main address 25 for Tx1, in Main address 24 for Tx2			1		dB
	D1 in Main address 25 for Tx1, in Main address 24 for Tx2			2		
	D2 in Main address 25 for Tx1, in Main address 24 for Tx2			4		
	D3 in Main address 25 for Tx1, in Main address 24 for Tx2			8		
	D4 in Main address 25 for Tx1, in Main address 24 for Tx2			16		
	D5 in Main address 25 for Tx1, in Main address 24 for Tx2			32		
Carrier Leakage	Relative to -3dBm output power; without calibration by modem sine and cosine signal applied to the I/Q baseband inputs			-40		dBc
Tx I/Q Input Impedance (RIIC)	Differential resistance			25		kΩ
	Differential capacitance			1		pF
Baseband Filter Rejection	3.5MHz channel bandwidth	2.33MHz		0.5		dB
		6.62MHz		45		
	5MHz channel bandwidth	3.33MHz		0.5		
		9.45MHz		45		
	7MHz channel bandwidth	4.67MHz		0.5		
		13.23MHz		45		
	10MHz channel bandwidth	6.67MHz		0.5		
		18.9MHz		45		
Baseband Group Delay Ripple	0 to 4.6MHz (BW = 10MHz)			10		ns
Baseband Input 1dB Gain Compression or Expansion	Sine and cosine signal applied to the I/Q baseband inputs, 5MHz I/Q inputs			0.5		V_{PEAK}
Isolation Between Tx Channel A and Tx Channel B				45		dB
Maximum Gain Mismatch Between Tx Channel A and Tx Channel B over RF Frequency	3.3GHz to 3.9GHz, single matching for entire band			±2		dB
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING POWER DETECTOR: Tx I/Q BASEBAND INPUT TO RECEIVER I-CHANNEL MULTIPLEXED OUTPUT						
Output AC-Coupling, -3dB Frequency				750		kHz
Baseband AC Amplifier Gain Range	Measure from minimum gain (D5:D4 = 00 in Main address 21) to maximum gain (D5:D4 = 11 in Main address 21)			30		dB

AC ELECTRICAL CHARACTERISTICS TABLE—Tx Mode (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{RF} = 3.601GHz, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, ENABLE = $\overline{CS}$ = high, TXRX = SCLK = DIN = low. Power matching at RF outputs using the *Typical Operating Circuit*. Lowpass filter is set to 10MHz RF channel BW; 90mV_{RMS}, 1MHz sine and cosine signal applied to I and Q baseband inputs of transmitter (differential DC-coupled). Registers set to default settings and corresponding test mode, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Ftone or 2Ftone Level at Output	Maximum - 2dB Tx gain (D5:D0 = 000010 in Main address 25 for Tx1, in Main address 24 for Tx2), -25dBc LO leakage, Ftone = 2MHz, and minimum AM detector gain (D5:D4 = 00 in Main address 21) (Note 3)		-17		dBm

AC ELECTRICAL CHARACTERISTICS TABLE—Frequency Synthesis

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, PLL loop bandwidth = 180kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN FREQUENCY SYNTHESIZER					
RF Channel Center Frequency Range		3.3		3.9	GHz
Channel Center Frequency Programming Minimum Step Size			25		Hz
Charge-Pump Comparison Frequency		19	44.8		MHz
Reference Frequency Range		19	44.8	80	MHz
Reference Frequency Input Levels	AC-coupled to REF_OSC pin	0.8			V_{P-P}
Reference Frequency Input Impedance (RIIC)	Resistance (REF_OSC pin)		10		kΩ
	Capacitance (REF_OSC pin)		1		pF
Programmable Reference Divider Values	D1:D0 = 00 in Local address 15		1		
	D1:D0 = 01 in Local address 15		2		
	D1:D0 = 10 in Local address 15		4		
Closed-Loop Integrated Phase Noise	Integrated phase noise from 200Hz to 5MHz		-38		dBc
Charge-Pump Output Current	On each differential side		0.8		mA
Spur Level	f_{OFFSET} = 0 to 1.8MHz		-40		dBc
	f_{OFFSET} = 44.8MHz		-77		
Turnaround LO Frequency Error	Relative to steady state; measured 35µs after Tx-Rx or Rx-Tx switching instant, and 4µs after any receiver gain changes		±50		Hz
Temperature Range over Which VCO Maintains Lock	Relative to the ambient temperature T_A, as long as the VCO lock temperature range is within operating temperature range		T_A ±40		°C
CLKOUT Divider Values	TXRX = 0 at the CLKOUTEN rising edge		1		
	TXRX = 1 at the CLKOUTEN rising edge		2		

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AC ELECTRICAL CHARACTERISTICS TABLE—Frequency Synthesis (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, PLL loop bandwidth = 180kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKOUT Output Swing	R= 10kΩ, C_{LOAD} = 5pF	D7:6 = 00 in Local address 9 with 44.8MHz clock output		2.56		V_{P-P}
		D7:6 = 11 in Local address 9 with 22.4MHz clock output		2.66		

AC ELECTRICAL CHARACTERISTICS TABLE—Miscellaneous Blocks

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PA BIAS VOLTAGE						
Output High Level	10mA source current			V_{CC} - 0.2		V
Output Low Level	10mA sink current			0.2		V
Turn-On Time	Excludes programmable delay of 0 to 6.3µs in steps of 0.45µs			200		ns
VCTCXO DAC						
Output Current	Source current	D5:D0 = 000000 in Main address 29		0		µA
		D5:D0 = 111111 in Main address 29		315		
Maximum Output Voltage				2.4		V
Step Size				5		µA
ON-CHIP TEMPERATURE SENSOR						
Digital Output Code	Read-out at DOUT pin through SPI	T_A = +25°C		10001		
		T_A = +85°C		11010		
		T_A = -40°C		00101		
Temperature Step Size				5		°C

AC ELECTRICAL CHARACTERISTICS TABLE—Timing

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode**,** PLL loop bandwidth = 180kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING							
Channel Switching Time		Frequency error settles to ±50Hz	Automatic VCO sub-band selection		2		ms
			Manual VCO sub-band selection		56		µs

AC ELECTRICAL CHARACTERISTICS TABLE—Timing (continued)

(MAX2842 Evaluation Kit, $V_{CC\_}$ = 2.7V to 3.6V, T_A = +25°C, f_{LO} = 3.6GHz, REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode**,** PLL loop bandwidth = 180kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turnaround Time		Measured from TXRX rising or falling edge; signal settling to within 0.5dB of steady state	Rx to Tx		2		µs
			Tx to Rx		2		
Tx Turn-On Time (From Standby Mode)		Measured from ENABLE rising edge; signal settling to within 0.5dB of steady state			2		µs
Tx Turn-Off Time (To Standby Mode)		From ENABLE falling edge			1		µs
Rx Turn-On Time (From Standby Mode)		Measured from ENABLE rising edge; signal settling to within 0.5dB of steady state			2		µs
Rx Turn-Off Time (To Standby Mode)		From ENABLE falling edge			1		µs
4-WIRE SERIAL PARALLEL INTERFACE TIMING (See Figure 1)							
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time	t_{CSO}				6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}				6		ns
DIN to SCLK Setup Time	t_{DS}				6		ns
DIN to SCLK Hold Time	t_{DH}				6		ns
SCLK Pulse-Width High	t_{CH}				6		ns
SCLK Pulse-Width Low	t_{CL}				6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time	t_{CSH}				6		ns
$\overline{CS}$ High Pulse Width	t_{CSW}				45		ns
Time Between Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK	t_{CS1}				6		ns
Clock Frequency	f_{CLK}					45	MHz
Rise Time	t_R				f_{CLK}/10		ns
Fall Time	t_F				f_{CLK}/10		ns
SCLK Falling Edge to Valid DOUT	t_D				12.5		ns

Note 1: MAX2842 ICs are production tested at T_A = +25°C. Min/max limits at T_A = -40°C and T_A = +85°C are guaranteed by design and characterization. There is **no** power-on register settings self-reset. Recommended register settings must be loaded after V_{CC} is applied.

Note 2: Loopback gain is production tested at $V_{CC\_}$ = 2.7V. Min/max limits over the supply voltage range are guaranteed by design and characterization.

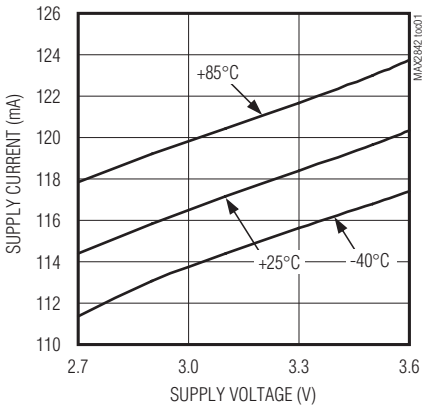
Note 3: The LO leakage produces Ftone, while the I/Q imbalance produces 2Ftone at the baseband output of the power detector. The output Ftone increases by 1dB for 1dB increase of the LO leakage, provided that the output power remains constant. The same relationship applies for the sideband leakage (due to I/Q imbalance) and 2Ftone.

3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

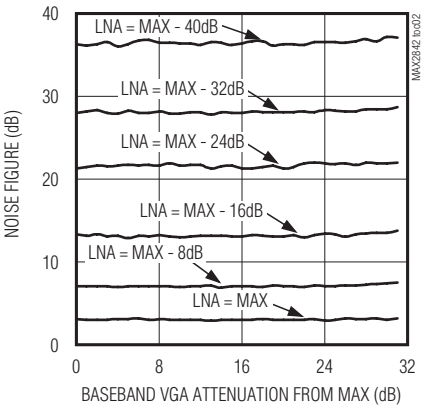
Typical Operating Characteristics

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

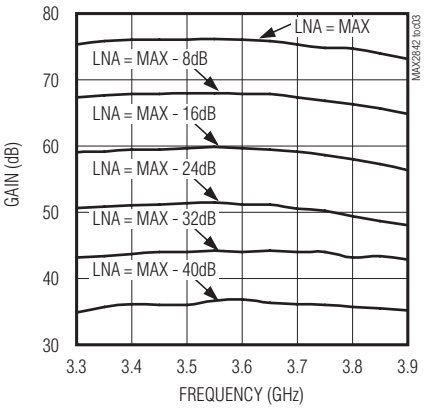
Rx SUPPLY CURRENT vs. SUPPLY VOLTAGE



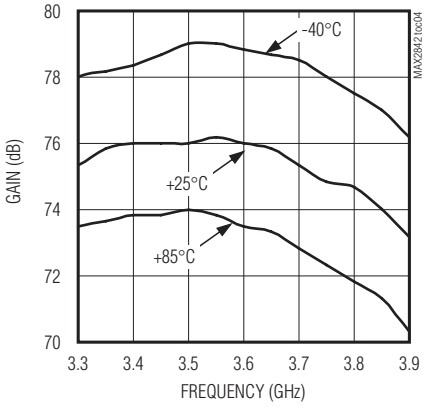
NOISE FIGURE vs. BASEBAND GAIN SETTING



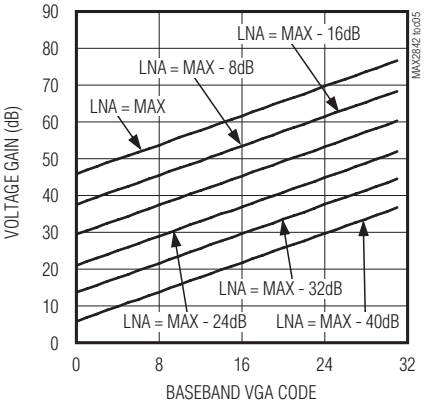
Rx VOLTAGE GAIN vs. FREQUENCY



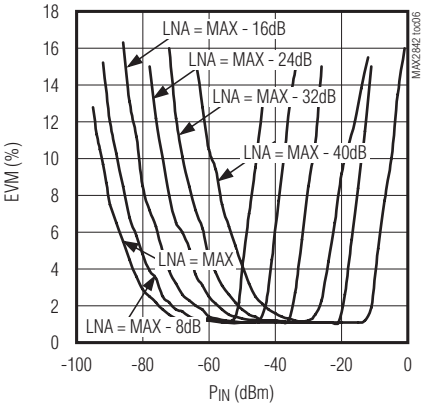
Rx VOLTAGE GAIN (MAXIMUM LNA GAIN) vs. FREQUENCY



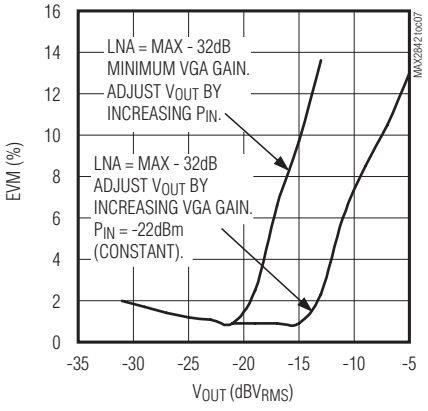
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



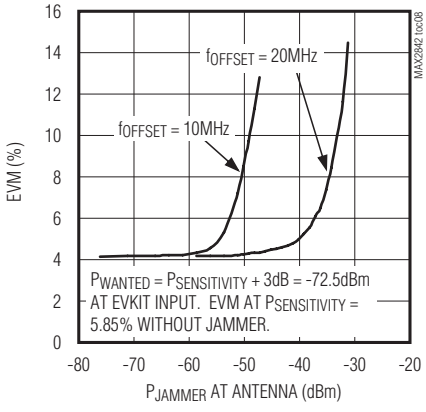
Rx EVM vs. P_{IN} (CHANNEL BANDWIDTH = 10MHz, 64-QAM FUSC)



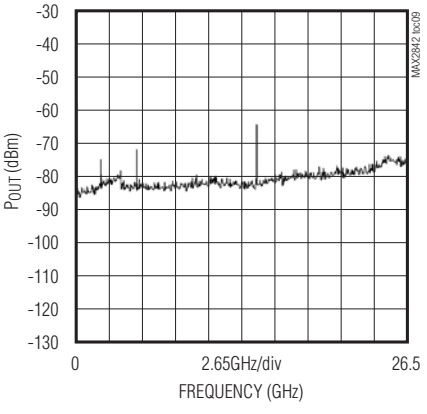
Rx EVM vs. V_{OUT} (CHANNEL BANDWIDTH = 10MHz, 64-QAM FUSC)



Rx EVM vs. OFDM JAMMER (10MHz CHANNEL BANDWIDTH, 64-QAM FUSC)



Rx EMISSION SPECTRUM, LNA INPUT (Tx OFF, LNA = MAX)

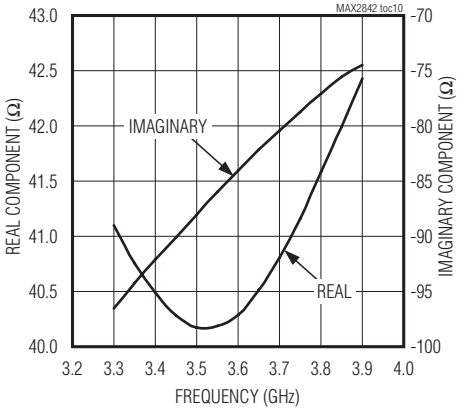


3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

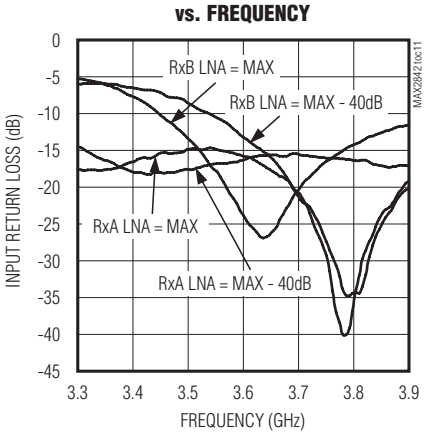
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

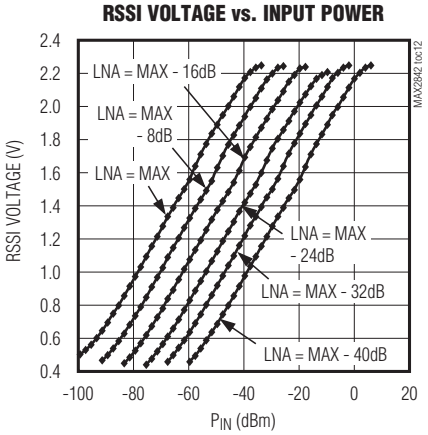
Rx INPUT DIFFERENTIAL IMPEDANCE vs. FREQUENCY



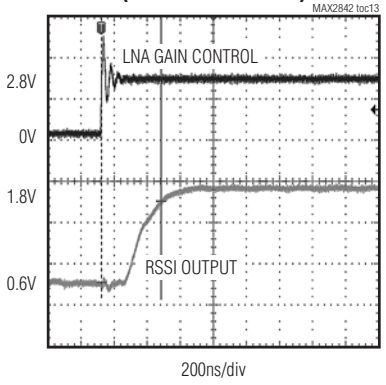
Rx INPUT RETURN LOSS vs. FREQUENCY



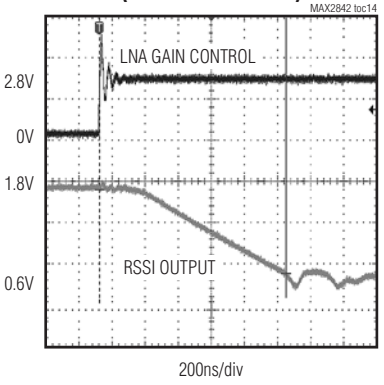
RSSI VOLTAGE vs. INPUT POWER



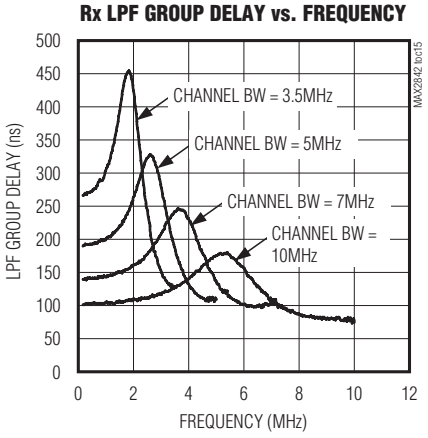
Rx RSSI STEP RESPONSE (+40dB SIGNAL STEP)



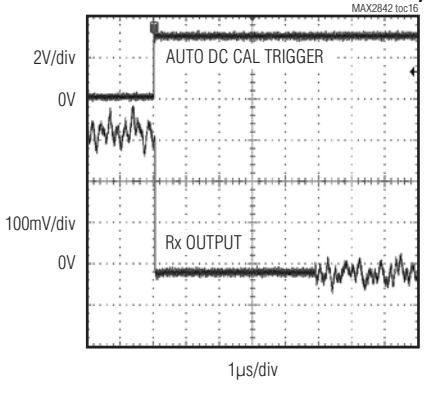
Rx RSSI STEP RESPONSE (-40dB SIGNAL STEP)



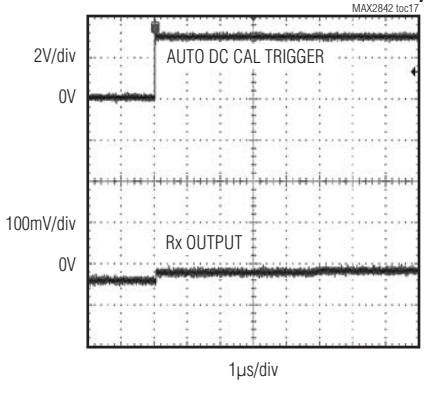
Rx LPF GROUP DELAY vs. FREQUENCY



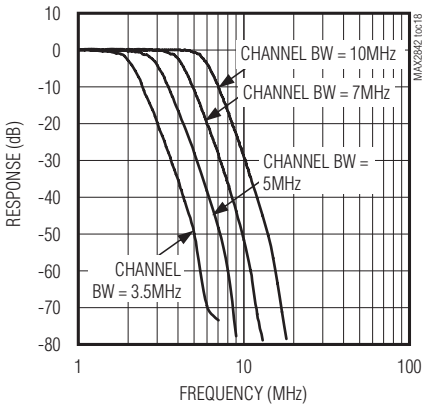
Rx DC OFFSET SETTING RESPONSE (TRIGGER AUTO DC CALIBRATION 400ns AFTER MIN TO MAX BB VGA GAIN STEP)



Rx DC OFFSET SETTING RESPONSE (TRIGGER AUTO DC CALIBRATION 400ns AFTER MAX TO MIN BB VGA GAIN STEP)



Rx BB FREQUENCY RESPONSE

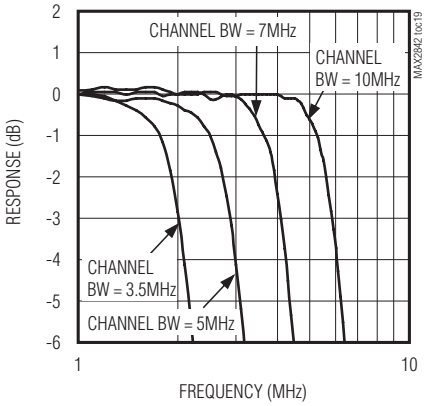


3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

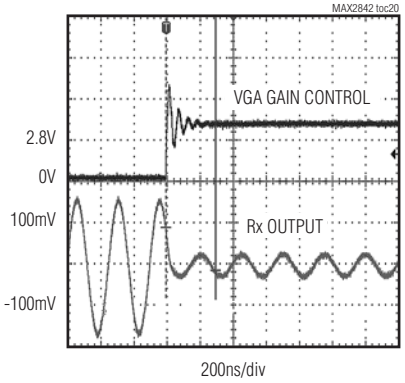
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

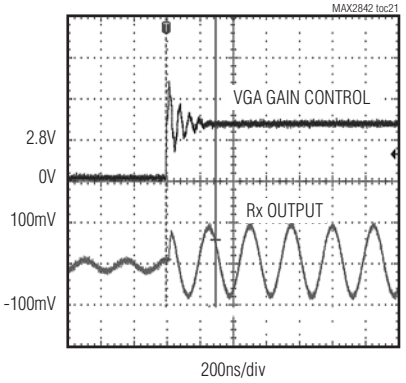
Rx BB FREQUENCY RESPONSE



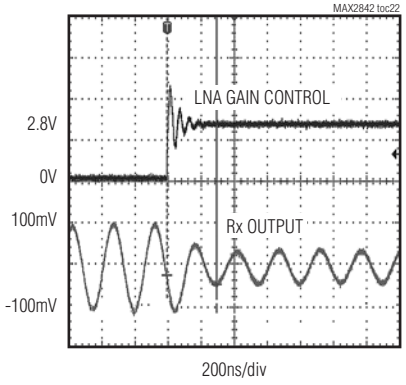
Rx VGA SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



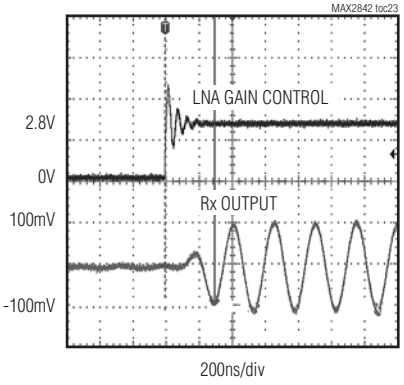
Rx VGA SETTLING RESPONSE (+16dB BB VGA GAIN STEP)



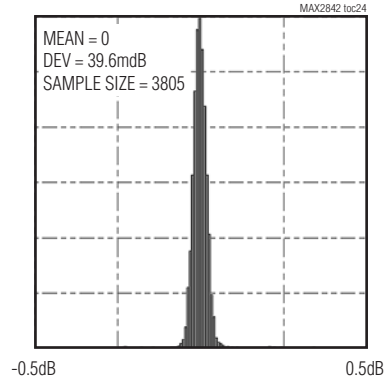
Rx LNA GAIN STEP SETTLING RESPONSE (MAX TO MIN - 8dB)



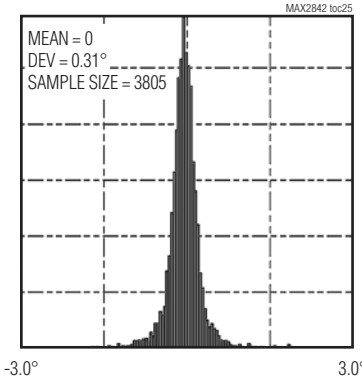
Rx LNA GAIN STEP SETTLING RESPONSE (MIN - 32 TO MAX)



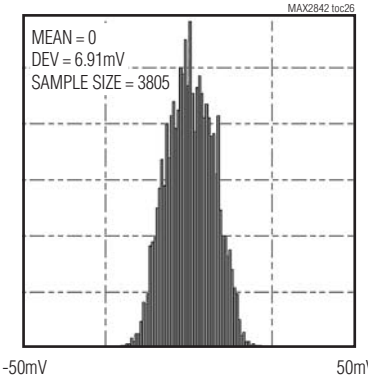
HISTOGRAM: Rx I/Q GAIN IMBALANCE



HISTOGRAM: Rx I/Q PHASE IMBALANCE



HISTOGRAM: Rx STATIC DC OFFSET

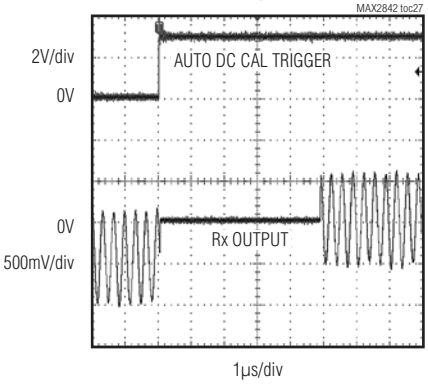


3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

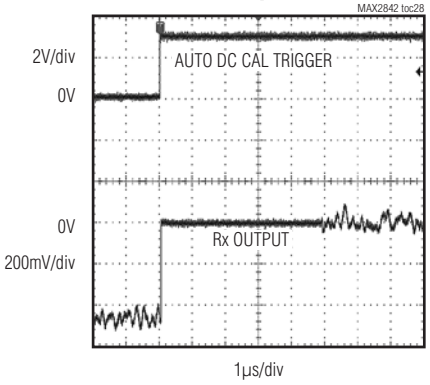
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

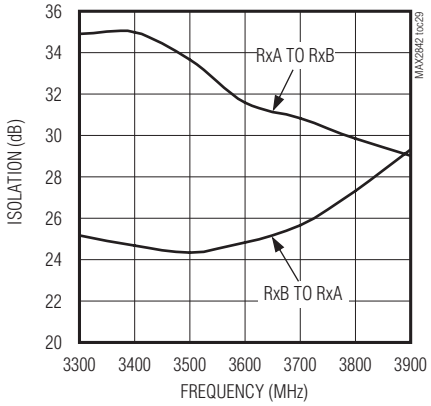
POWER-ON DC OFFSET CANCELLATION WITH INPUT SIGNAL (TRIGGER AUTO DC CALIBRATION 1µs AFTER ENABLE)



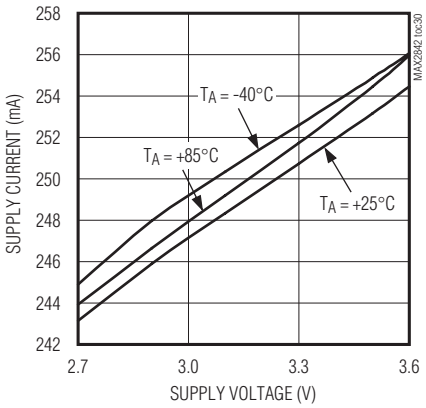
POWER-ON DC OFFSET CANCELLATION WITHOUT INPUT SIGNAL (TRIGGER AUTO DC CALIBRATION 1µs AFTER ENABLE)



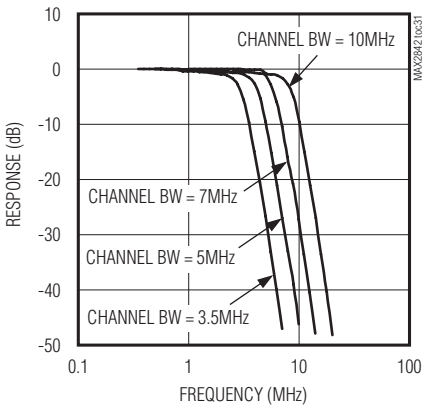
Rx ISOLATION vs. FREQUENCY



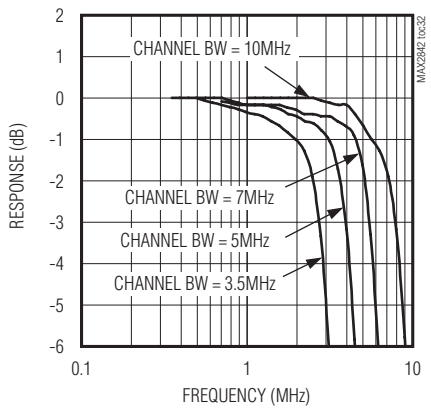
Tx SUPPLY CURRENT vs. SUPPLY VOLTAGE



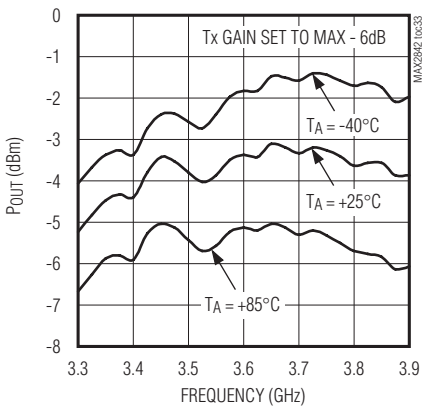
Tx BASEBAND FREQUENCY RESPONSE



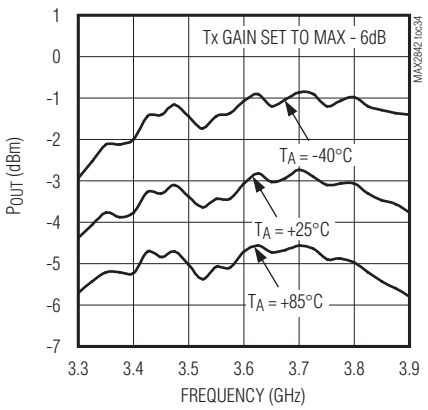
Tx BASEBAND FREQUENCY RESPONSE



TxA OUTPUT POWER vs. FREQUENCY



TxB OUTPUT POWER vs. FREQUENCY

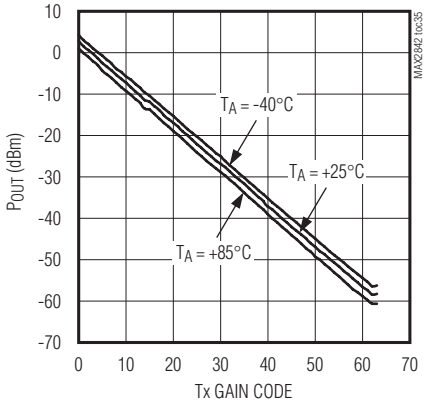


3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

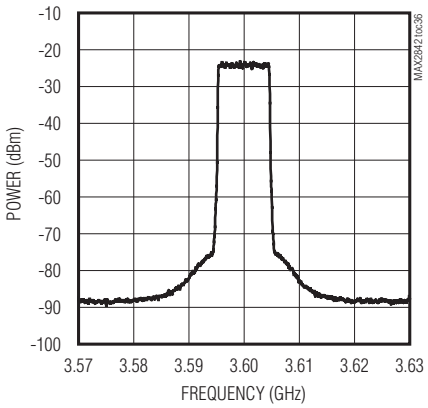
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

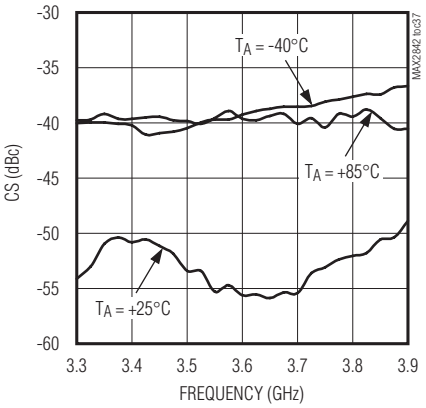
Tx OUTPUT POWER vs. GAIN SETTING



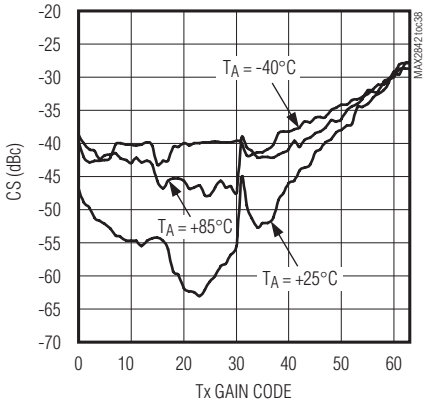
Tx OUTPUT SPECTRUM



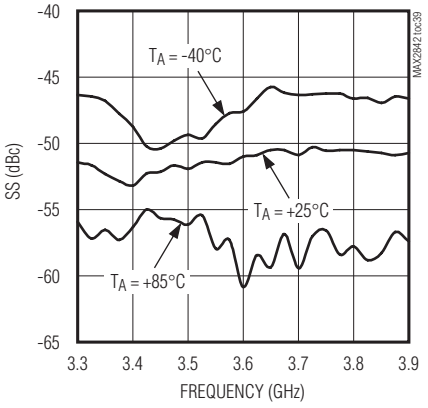
Tx CARRIER SUPPRESSION vs. FREQUENCY



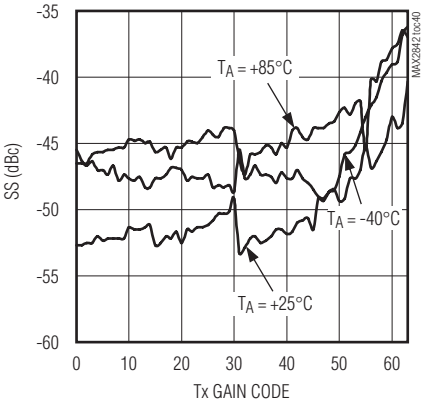
Tx CARRIER SUPPRESSION vs. GAIN SETTING



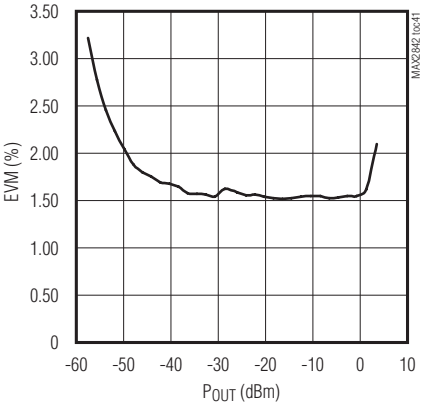
Tx SIDEBAND SUPPRESSION vs. FREQUENCY



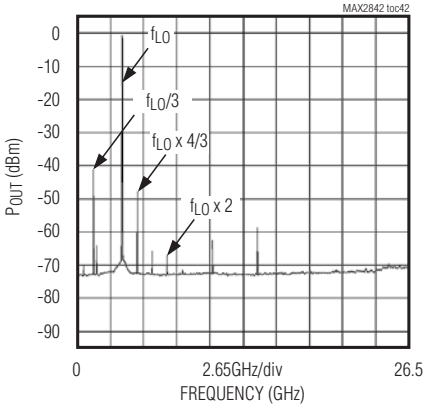
Tx SIDEBAND SUPPRESSION vs. GAIN SETTING



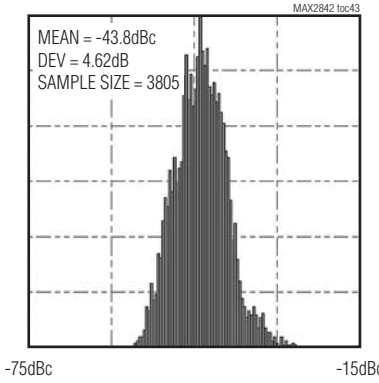
EVM vs. Tx OUTPUT POWER (64-QAM FUSC, 10MHz CHANNEL BANDWIDTH)



Tx OUTPUT EMISSION SPECTRUM



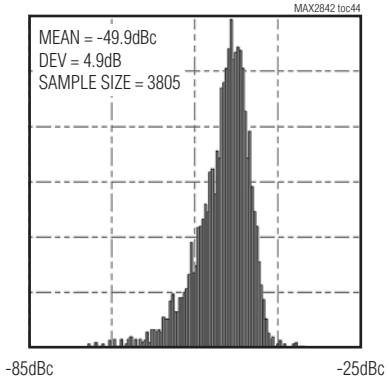
HISTOGRAM: Tx LO LEAKAGE



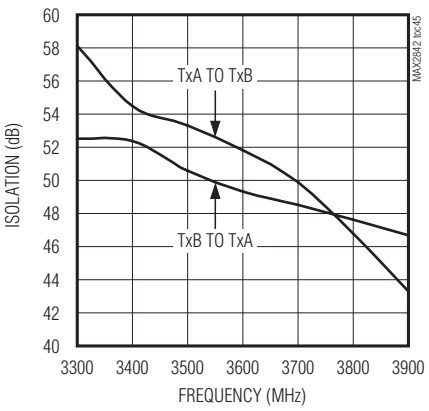
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

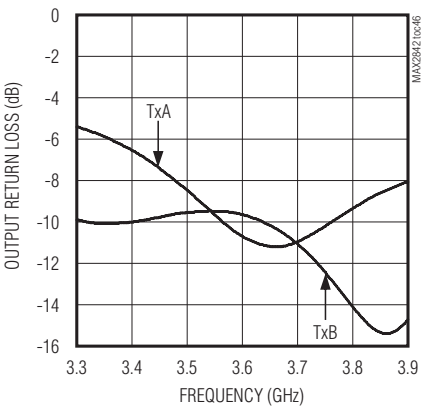
HISTOGRAM: Tx SIDEBAND SUPPRESSION



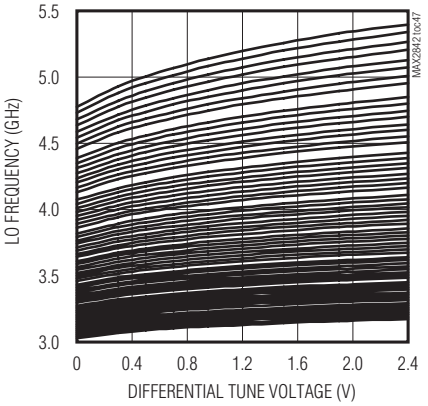
Tx ISOLATION vs. FREQUENCY



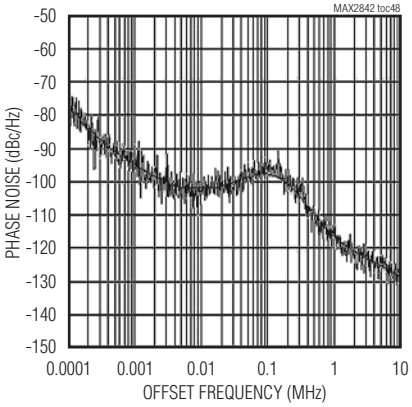
Tx OUTPUT RETURN LOSS vs. FREQUENCY



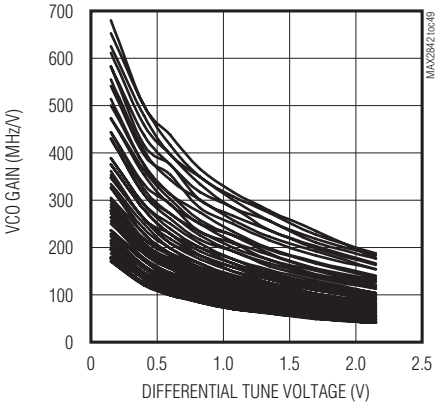
LO FREQUENCY vs. DIFFERENTIAL TUNE VOLTAGE



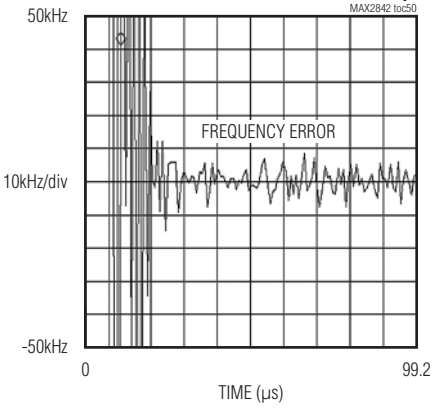
PHASE NOISE vs. OFFSET FREQUENCY



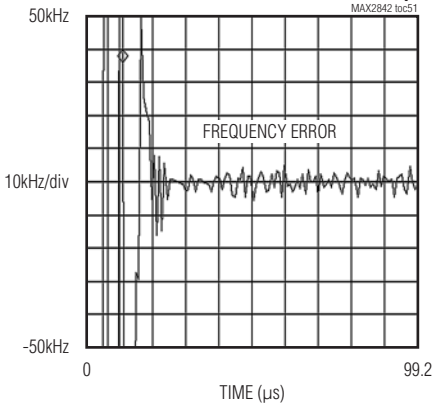
VCO GAIN vs. DIFFERENTIAL TUNE VOLTAGE



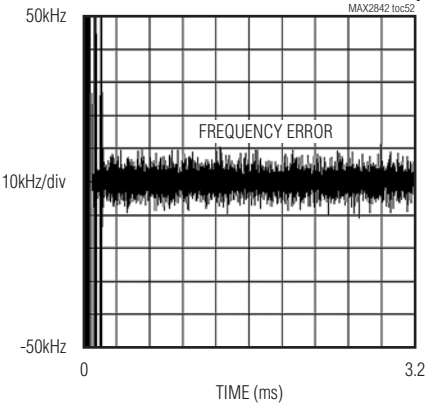
CHANNEL-SWITCHING FREQUENCY SETTLING (3.3GHz TO 3.9GHz, MANUAL VCO SUB-BAND SELECTION)



CHANNEL-SWITCHING FREQUENCY SETTLING (3.9GHz TO 3.3GHz, MANUAL VCO SUB-BAND SELECTION)



CHANNEL-SWITCHING FREQUENCY SETTLING (3.3GHz TO 3.9GHz, AUTOMATIC VCO SUB-BAND SELECTION)

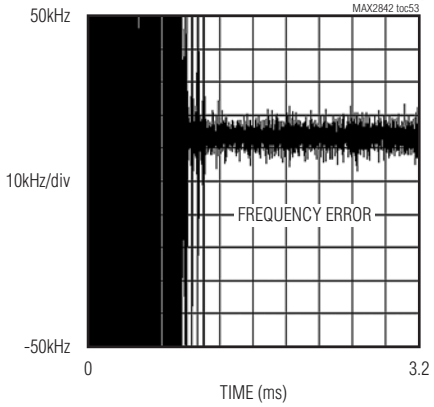


3.3GHz to 3.9GHz MIMO Wireless Broadband RF Transceiver

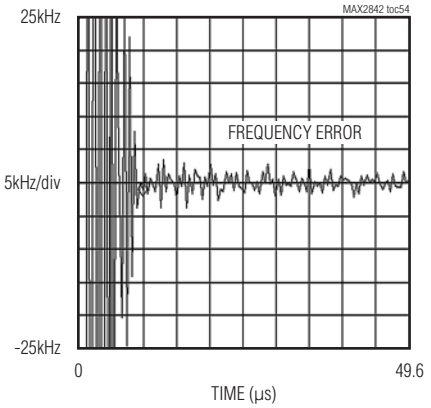
Typical Operating Characteristics (continued)

($V_{CC\_}$ = 2.8V, T_A = +25°C, f_{LO} = 3.6GHz, f_{REF} = REF_OSC frequency = 44.8MHz, $\overline{CS}$ = high, SCLK = DIN = low, ENABLE and TXRX logic inputs as per operating mode, RF BW = 10MHz, Tx output at 50Ω unbalanced output of balun, using the MAX2842 Evaluation Kit.)

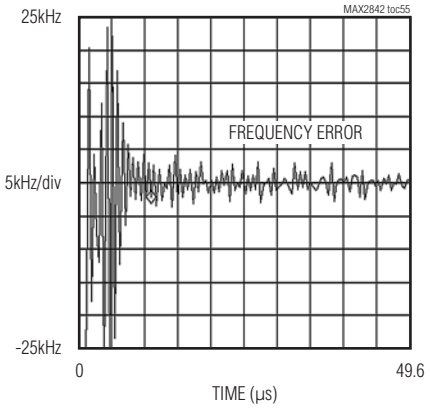
CHANNEL-SWITCHING FREQUENCY SETTLING (3.9GHz TO 3.3GHz, AUTOMATIC VCO SUB-BAND SELECTION)



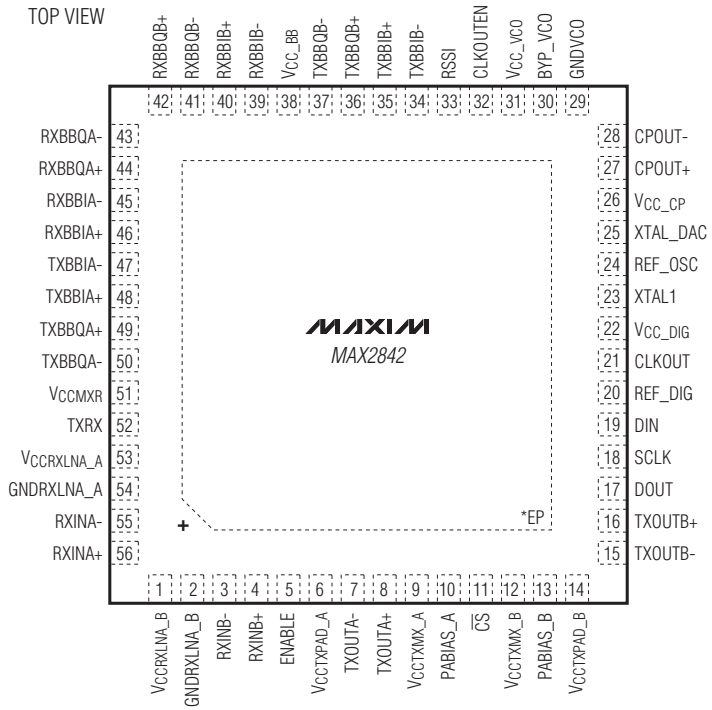
Rx-TO-Tx TURNAROUND FREQUENCY GLITCH SETTLING



Tx-TO-Rx TURNAROUND FREQUENCY GLITCH SETTLING



Pin Configuration



THIN QFN 7mm x 7mm

*EXPOSED PADDLE.

Pin Description

PIN	NAME	FUNCTION
1	$V_{CCRXLNA\_B}$	Receiver B LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
2	GNDRXLNA_B	Receiver B LNA Ground
3	RXINB-	Receiver B LNA Differential Input. Inputs are internally DC-coupled. Two external series capacitors and one shunt inductor match the inputs to 100Ω differential.
4	RXINB+	
5	ENABLE	Mode Control Logic Input. See Table 1 for operating modes.
6	$V_{CCTXPAD\_A}$	Transmitter A Supply Voltage for Transmitter Power-Amplifier Driver. Bypass with a capacitor as close as possible to the pin.
7	TXOUTA-	Transmitter A Power-Amplifier Driver Differential Output. The pins are internally DC-coupled. Two external series capacitors and one shunt inductor match the outputs to 100Ω differential.
8	TXOUTA+	
9	V_{CCTXMX_A}	Transmitter A Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
10	PABIAS_A	Transmit A External PA Bias Voltage Output
11	$\overline{CS}$	Chip-Select Logic Input of 4-Wire Serial Interface (See Figure 1)
12	V_{CCTXMX_B}	Transmitter B Upconverter Supply Voltage. Bypass with a capacitor as close as possible to the pin.
13	PABIAS_B	Transmit B External PA Bias Voltage Output
14	$V_{CCTXPAD\_B}$	Transmitter B Supply Voltage for Transmitter Power-Amplifier Driver. Bypass with a capacitor as close as possible to the pin.
15	TXOUTB-	Transmitter B Power-Amplifier Driver Differential Output. The pins are internally DC-coupled. Two external series capacitors and one shunt inductor match the outputs to 100Ω differential.
16	TXOUTB+	
17	DOUT	Data Logic Output of 4-Wire Serial Interface (See Figure 1)
18	SCLK	Serial-Clock Logic Input of 4-Wire Serial Interface (See Figure 1)
19	DIN	Data Logic Input of 4-Wire Serial Interface (See Figure 1)
20	REF_DIG	CMOS Logic Supply-Voltage Reference Input. Bypass with a capacitor as close as possible to the pin. It is tested at 2.7V and 3.6V. For 1.8V voltage support, contact the manufacturer.
21	CLKOUT	Divided Reference Clock Output
22	V_{CC_DIG}	Digital Blocks Supply Voltage. Bypass with a capacitor as close as possible to the pin.
23	XTAL1	Crystal Connection. (If the on-chip crystal oscillator is not used, leave this input unconnected.)
24	REF_OSC	44.8MHz Reference Clock Input or Crystal Connection. AC-couple a crystal or a reference clock to this analog input.
25	XTAL_DAC	Source Current DAC Output for VCTCXO
26	V_{CC_CP}	PLL Charge-Pump Supply Voltage. Bypass with a capacitor as close as possible to the pin.
27	CPOUT+	Differential Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT+ and CPOUT- (see the *Typical Operating Circuit*).
28	CPOUT-	
29	GNDVCO	VCO Ground
30	BYP_VCO	On-Chip VCO Regulator Output Bypass. Bypass with a 1µF capacitor to GND. Do not connect other circuitry to this point.
31	V_{CC_VCO}	VCO Supply Voltage. Bypass with a capacitor as close as possible to the pin.
32	CLKOUTEN	Logic Input to Enable CLKOUT
33	RSSI	RSSI or Temperature Sensor Multiplexed Analog Output
34	TXBBIB-	Transmitter B Baseband I-Channel Differential Inputs
35	TXBBIB+	
36	TXBBQB+	Transmitter B Baseband Q-Channel Differential Inputs
37	TXBBQB-	

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Pin Description (continued)

PIN	NAME	FUNCTION
38	V_{CC_BB}	Receiver Baseband Supply Voltage. Bypass with a capacitor as close as possible to the pin.
39	RXBBIB-	Receiver B Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
40	RXBBIB+	
41	RXBBQB-	Receiver B Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
42	RXBBQB+	
43	RXBBQA-	Receiver A Baseband Q-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
44	RXBBQA+	
45	RXBBIA-	Receiver A Baseband I-Channel Differential Outputs. In Tx calibration mode, these pins are the LO leakage and sideband detector outputs.
46	RXBBIA+	
47	TXBBIA-	Transmitter A Baseband I-Channel Differential Inputs
48	TXBBIA+	
49	TXBBQA+	Transmitter A Baseband Q-Channel Differential Inputs
50	TXBBQA-	
51	V_{CCMXR}	Receiver Downconverters Supply Voltage. Bypass with a capacitor as close as possible to the pin.
52	TXRX	Mode Control Logic Input. See Table 1 for operating modes.
53	$V_{CCRXLNA\_A}$	Receiver A LNA Supply Voltage. Bypass with a capacitor as close as possible to the pin.
54	GNDRXLNA_A	Receiver A LNA Ground
55	RXINA-	Receiver A LNA Differential Input. Inputs are internally DC-coupled. Two external series capacitors and one shunt inductor match the inputs to 100Ω differential.
56	RXINA+	
—	EP (GND)	Exposed Paddle Ground. Internally connected to ground. Connect to a large ground plane for optimum RF performance and enhanced thermal dissipation. Do not share with other pin grounds and bypass capacitors' ground.

Table 1. Operating Mode Table

	MODE CONTROL LOGIC INPUTS				CIRCUIT BLOCK STATES				
MODE	**SPI MAIN REGISTER 22, D1:D0 (Note 1)**	**ENABLE PIN**	**TXRX PIN**	**CLKOUTEN PIN**	**Rx PATH**	**Tx PATH**	**PLL, VCO**	**CLOCK OUT**	**CALIBRATION SECTIONS ON**
SHUTDOWN	00	0	0	0	Off	Off	Off	Off	None
CLKOUT (Note 2)	00	0	0	1	Off	Off	Off	On	None
STANDBY	01	0	1	X	Off	Off (Note 3)	On	On/Off	None
Rx (Note 4)	01	1	1	X	On	Off	On	On/Off	None
Tx (Note 5)	01	1	0	X	Off	On	On	On/Off	None
Tx Calibration (Notes 6, 7)	11	1	0	X	Off	On (except PA driver)	On	On/Off	AM detector + Rx I/Q buffers
Rx Calibration	11	1	1	X	On (except LNA)	On (except PA driver)	On	On/Off	Loopback

X = Don't care.

Note 1: State "10" of SPI Main register 22, D1:D0 is the same as state "00" but not tested, and therefore should not be used.
Note 2: CLKOUT signal is active independent of the states of SPI register 22, D1:D0. Clock divide ratio and on-chip crystal oscillator are configured by different pins during power-up or rising edge of CLKOUTEN pin. See the *Clock-Out Only Mode* section in the *Detailed Description* for details.
Note 3: PA bias blocks may be selectively enabled in all modes except SHUTDOWN and CLKOUT.
Note 4: Set Main register 0, D5 = 1 to enable both RxA and RxB. Set Main register 0, D5 = 0 to enable only RxA.
Note 5: Set Main register 22, D2 = 1 to enable both TxA and TxB. Set Main register 22, D2 = 0 to enable only TxA.
Note 6: Set SPI Main register 6, D9 = 1 to mux AM detector output to RXBB_ pins.
Note 7: Set SPI Main register 22, D3 = 1 to calibrate TxA; set Main register 22, D3 = 0 to calibrate TxB.

Detailed Description

Modes of Operation

The modes of operation for the MAX2842 are shutdown, clock-out, standby, Tx, Rx, Tx calibration, and Rx calibration. See Table 1 for a summary of the modes of operation. The logic input pins—TXRX (pin 52) and ENABLE (pin 5)—control the various modes.

Shutdown Mode

Current drain is the minimum possible with the supply voltages applied. All circuit blocks are powered down, except the 4-wire serial bus and its internal programmable registers. If the digital supply voltage is applied at the V_{CCDIG} pin, the registers may be loaded.

Clock-Out Only Mode

Only the clock-out signal is active on the CLKOUT pin. The clock output divider is also functional. The rest of the transceiver is powered down.

The reference and CLKOUT can be configured by different pins (ENABLE, TXRX, DIN, and $\overline{CS}$) at the rising edge of the CLKOUTEN pin. After the rising edge of the CLKOUTEN pin, all logic pins will not change the state of the crystal oscillator and CLKOUT signal. Table 2 summarizes how different parameters are configured.

For operation that does **not** need CLKOUT to be available, the reference buffer/crystal oscillator can be configured at the CLKOUTEN rising edge. The CLKOUT signal can then be disabled by applying CLKOUTEN = "0."

Standby Mode

PLL, VCO, and LO Gen blocks are generally on, so that Tx or Rx modes can be quickly enabled from this mode. These and other blocks may be selectively enabled or disabled in this mode. CLKOUT is enabled using the CLKOUTEN pin.

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Table 2. CLKOUT Divide Ratio, Crystal Oscillator/Reference Buffer, and Oscillator Bias Selection During CLKOUTEN Pin Rising Edge*

PIN	LEVEL	SELECT	NOTE
TXRX at CLKOUTEN Rising Edge	0	Divide-by-1	—
	1	Divide-by-2	—
ENABLE at CLKOUTEN Rising Edge	0	Disable on-chip crystal oscillator	Works as a reference buffer
	1	Enable on-chip crystal oscillator	—
$\overline{CS}$, DIN at CLKOUTEN Rising Edge (Only Needed When Crystal Oscillator Is Active)	11	40MHz	50Ω max
		38.4MHz	50Ω max
		52MHz	50Ω max
		44.8MHz	50Ω max

**The above selection cannot be programmed through SPI.*

Rx Mode

All Rx circuit blocks are powered on and active. The antenna signal is applied; RF is downconverted, filtered, and buffered at the Rx baseband I and Q outputs. The slow-charging Tx circuits are in a precharged "idle-off" state for fast Rx-to-Tx turnaround time. CLKOUT is enabled using the CLKOUTEN pin.

Tx Mode

All Tx circuit blocks are powered on. The external PA is powered on after a programmable delay. The Tx driver amplifier is ramped from the low-gain state (minimum RF output) to the programmed high-gain state. The slow-charging Rx circuits are in a precharged "idle-off" state for fast Tx-to-Rx turnaround time. CLKOUT is enabled using the CLKOUTEN pin.

Tx Calibration Mode

All Tx circuit blocks except the PA driver and external PA are powered on and active. The AM detector and receiver I/Q channel buffers are also on, along with multipexers in the receiver side to route this AM detector's signal to each I and Q differential line. The output of the Tx VGA is fed to the AM detector, so the PA driver gain steps will not affect this calibration signal path gain. CLKOUT is enabled using the CLKOUTEN pin.

Rx Calibration Mode

Part of the Rx and Tx circuit blocks, except the LNA and PA driver, are powered on and active. The transmitter I/Q input signal is upconverted to RF, and at the output of the Tx gain control (VGA) it is fed to the receiver at the input of the downconverter. Either or both of the two receiver channels can be connected to the transmitter and powered on. The I/Q lowpass filters are not present in the transmitter signal path (they are bypassed). The PA driver gain steps (part of the Tx gain control range) are not intended to affect the loopback signal level. CLKOUT is enabled using the CLKOUTEN pin.

Power-On Sequences

To ensure proper operation from power-down, the user needs to:

1) Enable the crystal oscillator, and wait at least 2ms.
2) Program the IC into standby mode and wait 2ms for frequency acquisition (56µs if manual VCO sub-band selection is used).
3) Program the IC into Rx or Tx mode for normal operation.
4) In Rx mode, the user needs to first trigger automatic DC calibration with SPI and wait 5µs for settling.

Programmable Registers and 4-Wire SPI Interface

The MAX2842 includes 55 programmable 16-bit registers. There are 32 Main registers and 23 Local registers. The most significant bit (MSB) is the read/write selection bit (R/W in Figure 1). The next 5 bits are a register address (A4:A0 in Figure 1). The 10 least significant bits (LSBs) are register data (D9:D0 in Figure 1). Register data is loaded through the 4-wire SPI/MICROWIRE™-compatible serial interface. The MSB of data at the DIN pin is shifted in first and is framed by $\overline{CS}$. When $\overline{CS}$ is low, the clock is active, and input data is shifted at the rising edge of the clock at the SCLK pin. At the $\overline{CS}$ rising edge, the 10-bit data bits are latched into the register selected by the address bits. See Figure 1. To support more than a 32-register address using a 5-bit wide address word, the bit 9 of address 0 is used to select whether the 5-bit

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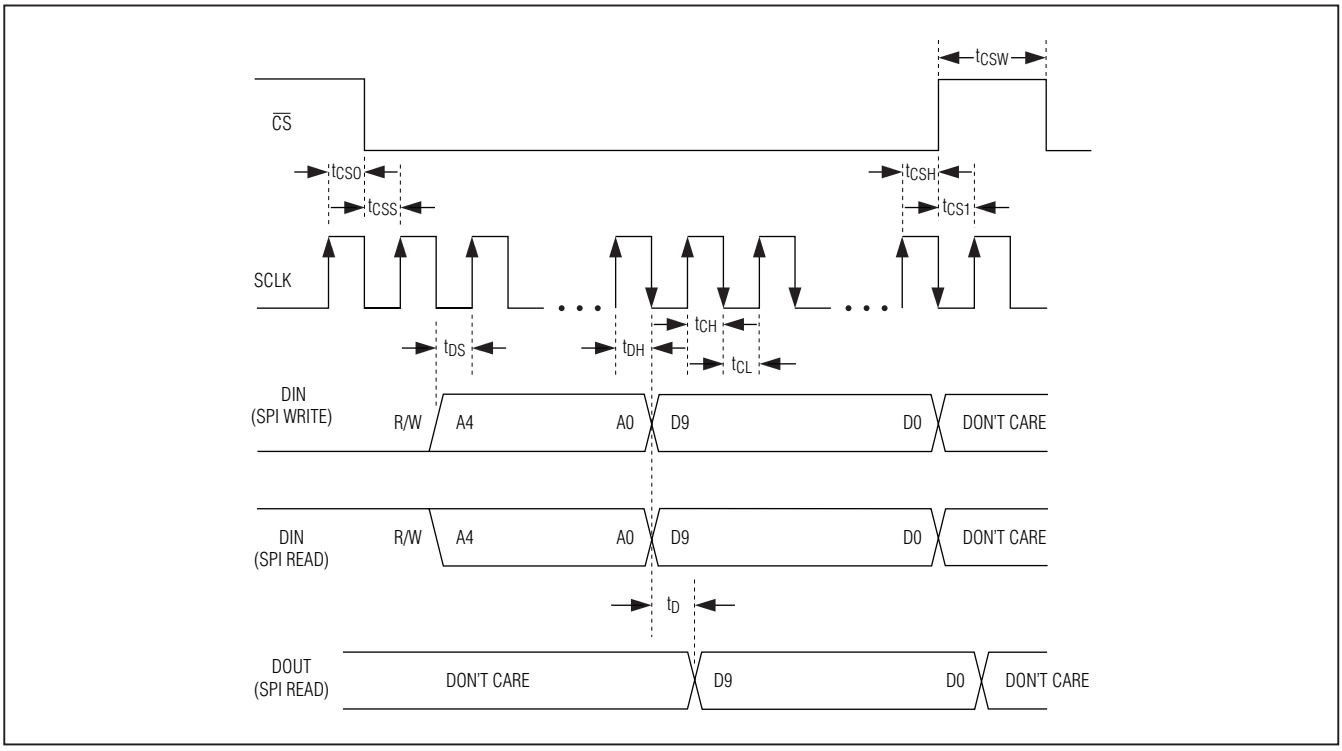

Figure 1. 4-Wire SPI Serial-Interface Timing Diagram

address word is applied to the main address or local address. The register values are preserved in shutdown mode as long as the power-supply voltage is maintained. There is **no** guaranteed power-on SPI register self-reset functionality in the MAX2842; the user must program all register values after power-up. During the read mode, register data selected by the address bits is shifted out to the DOUT pin at the falling edges of the clock.

SPI Register Definition

All values in register definition tables are typical numbers. The MAX2842 SPI does not have a power-on-default self-reset feature; the user must program all SPI addresses for normal operation. Prior to the use of any untested settings, contact the factory.

Table 3. MAX2842 Register Summary

REGISTER	WRITE/READ AND ADDRESS			DATA									
	MAIN0 D9	A4:A0	WRITE/ READ	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main0	0	00000	W/R	SPI_ program_ sel	RSSI_ Rxsel_SPI	RSSI_MUX*	RESERVED	MIMO_ mode_sel	ts_en	ts_adc_ trigger	FT[1:0]		LNAband
			Default	0	1	0	0	1	0	0	1	1	0
Main1	0	00001	Default	0	0	0	0	0	0	0	0	0	0
Main2	0	00010	W/R	dccal_ word_sel_A*	RESERVED	VGA1[4:0]					LNA1_GAIN[2:0]		
			Default	0	1	1	1	1	1	1	0	0	0

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Table 3. MAX2842 Register Summary (continued)

REGISTER	WRITE/READ AND ADDRESS			DATA									
	MAIN0 D9	A4:A0	WRITE/ READ	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main3	0	00010	W/R	dccal_ word_sel_B	RESERVED	VGA2[4:0]					LNA2_GAIN[2:0]		
			Default	0	1	1	1	1	1	1	0	0	0
Main4	0	00100	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	lclkdiv*	RESERVED	RESERVED
			Default	0	0	0	1	0	0	1	1	0	0
Main5	0	00101	Default	1	1	0	0	0	0	0	0	0	0
Main6	0	00110	W/R	sel_In1_In2	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	0	0	0	0	0	0	0	0
Main7	0	00111	W/R	gain_ cntrl_2RX	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	0	0	0	0	0	0	0	0
Main8	0	01000	Default	0	1	0	0	0	0	0	0	0	0
Main9	0	01001	Default	1	1	0	0	0	0	0	0	0	0
Main10	0	01010	W/R	dccal_ auto_en	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	0	0	0	0	0	0	0	0
Main11	0	01011	Default	0	1	0	0	0	0	0	0	0	0
Main12	0	01100	Default	0	1	0	0	0	0	0	0	0	0
Main13	0	01101	Default	0	0	0	0	0	0	0	0	0	0
Main14	0	01110	Default	0	0	0	0	0	0	0	0	0	0
Main15	0	01111	Default	0	0	0	0	0	0	0	0	0	0
Main16	0	10000	Default	0	0	0	0	0	0	0	0	0	0
Main17	0	10001	Default	0	0	0	0	0	0	0	0	0	0
Main18	0	10010	Default	0	0	0	0	0	0	0	0	0	0
Main19	0	10011	Default	0	0	0	0	0	0	0	0	0	0
Main20	0	10100	Default	0	0	0	0	0	0	0	0	0	0
Main21	0	10101	W	RESERVED	RESERVED	RESERVED	RESERVED	TXCAL_GAIN[1:0]		RESERVED	RESERVED	RESERVED	RESERVED
			R	DIE_ID[2:0]			REVISION_ID[2:0]						
			Default	0	0	1	1	0	0	0	0	0	0
Main22	0	10110	W/R	RESERVED	RESERVED	DOUT_SEL[2:0]			DOUT_ CSB_SEL*	TX_AMD_ SEL	TX_MIMO_ SEL	CAL_SPI	EN_SPI
			Default	0	0	0	0	0	0	0	1	0	0
Main23	0	10111	Default	0	0	1	0	0	0	0	0	0	0
Main24	0	11000	W/R	PABIAS_ VMODE_B	PABIAS_ TX_EN_B	RESERVED	RESERVED	TXGAIN_SPI_B[5:0]					
			Default	1	0	0	0	1	1	1	1	1	1
Main25	0	11001	W/R	PABIAS_ VMODE_A	PABIAS_ TX_EN_A	RESERVED	RESERVED	TXGAIN_SPI_A[5:0]					
			Default	1	0	0	0	1	1	1	1	1	1

Table 3. MAX2842 Register Summary (continued)

REGISTER	WRITE/READ AND ADDRESS			DATA									
	MAIN0 D9	A4:A0	WRITE/ READ	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Main26	0	11010	W/R	SYN_CONFIG0[9:0]									
			Default	0	1	0	1	0	1	0	1	0	1
Main27	0	11011	W/R	SYN_CONFIG0[19:10]									
			Default	0	1	0	1	0	1	0	1	0	1
Main28	0	11100	W/R	VAS_ TRIG_EN*	SYN_CONFIG1[8:0]								
			Default	1	0	0	1	1	1	0	1	0	0
Main29	0	11101	W/R	RESERVED	RESERVED	XTAL_TUNE[7:0]							
			Default	1	0	0	0	0	0	0	0	0	0
Main30	0	11110	W	LOGEN_BAND[1:0]		VAS_ RELOCK_ SEL*	VAS_MODE	VAS_SPI[5:0]					
			R		VAS_ADC[2:0]			VCO_BSW[5:0]					
			Default	0	1	0	1	0	1	1	1	1	1
Main31	0	11111	Default	1	1	1	1	0	1	0	1	0	0
Local1	1	00001	Default	1	0	0	0	0	0	0	0	0	0
Local2	1	00010	Default	0	0	0	0	0	0	0	0	0	1
Local3	1	00011	Default	1	0	1	0	0	1	1	0	1	0
Local4	1	00100	Default	0	1	0	0	0	0	0	0	1	0
Local5	1	00101	Default	0	1	1	0	1	1	0	0	0	0
Local6	1	00110	Default	0	0	1	0	0	0	0	0	0	0
Local7	1	00111	W	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED					
			R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	ts_adc[4:0]				
			Default	0	0	0	0	0	0	0	0	0	0
Local8	1	01000	Default	1	0	0	0	0	0	0	1	0	1
Local9	1	01001	W/R	RESERVED	XTAL_ DAC_EN	CLKOUT_DRV[1:0]		RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	1	0	0	0	0	0	1	1	1	1
Local10	1	01010	Default	0	0	0	1	0	0	1	0	1	1
Local11	1	01011	Default	0	0	0	0	0	1	0	0	0	0
Local12	1	01100	Default	0	0	1	0	0	0	0	0	0	0
Local13	1	01101	Default	0	0	0	0	0	0	0	0	0	0
Local14	1	01110	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PADAC_ DIVH*	PADAC_DLY[3:0]			
			Default	0	0	1	0	1	1	0	0	1	1
Local15	1	01111	W/R	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	LOGEN_ 2GM	RESERVED	RESERVED	REF_DIV[1:0]	
			Default	1	1	0	1	0	0	0	1	0	

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Table 3. MAX2842 Register Summary (continued)

REGISTER	WRITE/READ AND ADDRESS			DATA									
	MAIN0 D9	A4:A0	WRITE/ READ	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Local16	1	10000	W/R	VAS_VCO_ READOUT	DIE_ID_ READ	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
			Default	0	1	0	0	0	0	0	0	0	0
Local17	1	10001	Default	0	0	0	0	0	0	1	0	0	0
Local18	1	10010	Default	0	0	0	0	0	0	0	0	0	0
Local19	1	10011	Default	0	0	0	0	0	0	0	0	0	0
Local20	1	10100	Default	0	0	0	0	0	0	0	0	0	0
Local21	1	10101	Default	0	0	0	0	0	0	0	0	0	0
Local26	1	11010	Default	0	0	0	0	0	0	0	0	1	1
Local27	1	11011	Default	0	0	0	0	1	0	0	0	0	1

**These bits are not production tested. For functionality support, contact the manufacturer.*

Table 4. Main Address 0 (A4:A0 = 00000)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
SPI_program_sel	D9	Select to program main or local registers for each address except for address 0. 0 = Program main registers (default) 1 = Program local registers
RSSI_RXsel_SPI	D8	Select RSSI input. 0 = Select input from RxB 1 = Select input from RxA (default)
RSSI_MUX	D7	RSSI pin output mux. This bit is not production tested. For functionality support, contact the manufacturer. 0 = RSSI (default) 1 = Temperature sensor
RESERVED	D6	Reserved bits—set to default
MIMO_mode_sel	D5	Rx MIMO mode selection. 0 = Only RxA is active 1 = Both RxA and RxB are active (default)
ts_en	D4	Temperature sensor comparator and clock enable. 0 = Disable (default) 1 = Enable
ts_adc_trigger	D3	Temperature sensor ADC trigger. 0 = Not trigger ADC read-out (default) 1 = Trigger ADC read-out. ADC is disabled automatically after read-out finishes.
FT[1:0]	D2:D1	LPF RF bandwidth. 00 = 3.5MHz 01 = 5.0MHz 10 = 7.0MHz 11 = 10.0MHz (default)
LNAband	D0	Select center frequency of LNA output LC tank. LNAband = 0 3.3GHz~3.6GHz (default) LNAband = 1 3.6GHz~3.9GHz

Table 5. Main Address 2 (A4:A0 = 00010, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
dccal_word_sel_A	D9	Select which VGA DC offset word to use for RxA. This bit is not production tested. For functionality support, contact the manufacturer. 0 = Use VGA DC offset word 1 (default) 1 = Use VGA DC offset word 2
RESERVED	D8	Reserved bits—set to default
VGA1[4:0]	D7:D3	Set attenuation in RxA VGA. 00000 = Minimum gain 00001 = Minimum gain + 1dB … 11111 = Maximum gain (default)
LNA1_GAIN[2:0]	D2:D0	RxA LNA gain-setting SPI controls. 000 = Maximum gain (default) 001 = -8dB from maximum gain 010 = -16dB from maximum gain 011 = -24dB from maximum gain 100 = Not tested 101 = Not tested 110 = -32dB from maximum gain 111 = -40dB from maximum gain

Table 6. Main Address 3 (A4:A0 = 00011, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
dccal_word_sel_B	D9	Select which VGA DC offset word to use for RxB. This bit is not production tested. For functionality support, contact the manufacturer. 0 = Use VGA DC offset word 1 (default) 1 = Use VGA DC offset word 2
RESERVED	D8	Reserved bits—set to default
VGA2[4:0]	D7:D3	Set attenuation in RxB VGA. 00000 = Minimum gain 00001 = Minimum gain + 1dB … 11111 = Maximum gain (default)
LNA2_GAIN[2:0]	D2:D0	RxB LNA gain-setting SPI controls. 000 = Maximum gain (default) 001 = -8dB from maximum gain 010 = -16dB from maximum gain 011 = -24dB from maximum gain 100 = Not tested 101 = Not tested 110 = -32dB from maximum gain 111 = -40dB from maximum gain

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Table 7. Main Address 4 (A4:A0 = 00100, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:3	Reserved bits—set to default
iclkdiv	D2	VGA DC offset calibration internal clock to external clock divide ratio. This bit is not production tested. For functionality support, contact the manufacturer. 0 = /1 (reference clock at or near 20MHz) 1 = /2 (reference clock at or near 40MHz, default)
RESERVED	D1:D0	Reserved bits—set to default

Table 8. Main Address 6 (A4:A0 = 00110, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
sel_In1_In2	D9	RXBBI_+/- and RXBBQ_+/- pin output select. 0 = Select Rx VGA output (default) 1 = Select Tx AM detector output
RESERVED	D8:D0	Reserved bits—set to default

Table 9. Main Address 7 (A4:A0 = 00111, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
gain_cntrl_2RX	D9	Select whether gain control word 1 in Main address 2 applies to both RxA and RxB, or to RxA only. 0 = Separate gain control is used (default) 1 = Gain of both RxA and RxB are controlled by gain word 1 (D7:D0) in Main address 2
RESERVED	D8:D0	Reserved bits—set to default

Table 10. Main Address 10 (A4:A0 = 01010, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
dccal_auto_en	D9	Auto DC calibration trigger. 0 = No change (default) 1 = Triggers autocalibration
RESERVED	D8:D0	Reserved bits—set to default

Table 11. Main Address 21 (A4:A0 = 10101, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
DIE_ID[2:0] (readback only)	D9:D7	Read die ID at Main address 21 D9:D7. Active when DIE_ID_READ (Main address 16 D8) = 1. 011 = MAX2842
REVISION_ID[2:0] (readback only)	D6:D4	Read revision ID at Main address 21 D6:D4. Active when DIE_ID_READ (Main address 16 D8) = 1. 000 = Pass1 001 = Pass2 …
TXCAL_GAIN[1:0]	D5:D4	Tx AM detector baseband gain control. 00 = Minimum gain (default) 01 = Minimum + 10dB 10 = Minimum + 20dB 11 = Minimum + 30dB
RESERVED	D3:D0	Reserved bits—set to default

Table 12. Main Address 22 (A4:A0 = 10110, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits—set to default
DOUT_SEL[2:0]	D7:D5	DOUT pin output mux select. If Local address 9 D4 = 0: 000 = SPI output (default) 001 = PLL lock detect. Valid when Local address 11 D3:D1 = 000. 010 = VAS test output by Main address 31 D9:D6
DOUT_CSB_SEL	D4	DOUT pin three-state control. This bit is not production tested. For functionality support, contact the manufacturer. 0 = DOUT pin is independent on $\overline{CS}$ pin (default) 1 = DOUT pin is three-state when $\overline{CS}$ is high
TX_AMD_SEL	D3	AM detector mux selection bit. Active when Tx calibration is on. 0 = Connect TxA to the AM detector circuitry (default) 1 = Connect TxB to the AM detector circuitry If Tx calibration is off, the AM detector is disconnected from both TxA and TxB.
TX_MIMO_SEL	D2	Tx MIMO mode selection. 0 = TxA is the only active transmitter 1 = Both TxB and TxA are active (default)
CAL_SPI	D1	Rx/Tx calibration mode enable. 0 = Normal operation (default) 1 = Calibration mode
EN_SPI	D0	Chip-enable bit. Logic AND with pin ENABLE to enable/disable the whole chip except the crystal oscillator and CLKOUT pin buffer. 0 = Disable (default) 1 = Enable

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Table 13. Main Address 24 (A4:A0 = 11000, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
PABIAS_VMODE_B	D9	PA bias voltage-mode output select of TxB. Active when TxB PA bias is on. 0 = Logic 0 output—set the output to GND 1 = Logic 1 output—set the output to V_{CC} (default) The output logics are swapped when TxB PA bias is off.
PABIAS_TX_EN_B	D8	TxB PA bias Tx enable. Enable TxB PA bias during TxB transmission. Turn-on delay is controlled by PADAC_DLY[3:0] (Local address 14 D3:D0). 0 = Disable (default) 1 = Enable when the TxB is transmitting
RESERVED	D7:D6	Reserved bits—set to default
TXGAIN_SPI_B[5:0]	D5:D0	TxB VGA SPI gain control. 000000 = Minimum attenuation … 111111 = Maximum attenuation (default)

Table 14. Main Address 25 (A4:A0 = 11001, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
PABIAS_VMODE_A	D9	PA bias voltage-mode output select of TxA. Active when TxA PA bias is on. 0 = Logic 0 output—set the output to GND 1 = Logic 1 output—set the output to V_{CC} (default) The output logics are swapped when TxA PA bias is off.
PABIAS_TX_EN_A	D8	TxA PA bias Tx enable. Enable TxA PA bias during TxA transmission. Turn-on delay is controlled by PADAC_DLY[3:0] (Local address 14 D3:D0). 0 = Disable (default) 1 = Enable when TxA is transmitting
RESERVED	D7:D6	Reserved bits—set to default
TXGAIN_SPI_A[5:0]	D5:D0	TxA VGA SPI gain control. 000000 = Minimum attenuation … 111111 = Maximum attenuation (default)

Table 15. Main Address 26 (A4:A0 = 11010, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
SYN_CONFIG0[9:0]	D9:D0	Synthesizer 20-bit fractional divide ratio bit [9:0]. Combine with Main address 27 D9:D0 to form the whole fractional word. Default = 0101010101

Table 16. Main Address 27 (A4:A0 = 11011, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
SYN_CONFIG0[19:10]	D9:D0	Synthesizer 20-bit fractional divide ratio bit [19:10]. Combine with Main address 26 D9:D0 to form the whole fractional word. Default = 0101010101

Table 17. Main Address 28 (A4:A0 = 11100, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
VAS_TRIG_EN	D9	VAS triggering by Main address 26 enable (see below description). This bit is not production tested. For functionality support, contact the manufacturer. 0 = Disable for small frequency adjustment (i.e., ~100kHz). 1 = Enable for channel switching (default)
SYN_CONFIG1[8:0]	D8:D0	Synthesizer 9-bit integer divide ratio. Default =001110100

Example: For an RF frequency of 3500MHz and PLL comparison frequency of 40MHz, the desired divide ratio is 3500 x (4/3)/40 = 116.666666. Signal SYN_CONFIG1[8:0] = 001110100 for integer 116. Signal SYN_CONFIG0[19:0] is programmed to 10101010101010101010 for fractional word 0.66666; it is stored in Main addresses 26 and 27.

Divide Ratio Program Sequence: When Main address 26 is programmed, the corresponding $\overline{CS}$ rising edge starts the follow actions:

1) Updates the previously programmed values of Main address 27 and 28.
2) Triggers the VCO autoselect (VAS) state machine (when Main address 28 D9 = 1).
   For correct operation, the PLL integer divider ratio must be changed first and VAS is then triggered. The recommended programming sequence is Main address 28 → Main address 27 → Main address 26.

Fine RF Frequency Adjustment: It is not desirable to retrigger the VAS/frequency acquisition if the user only changes the RF frequency by 100kHz or less. Program Main address 28 D9 = 0 to not trigger VAS after programming Main address 26.

Table 18. Main Address 29 (A4:A0 = 11101, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D8	Reserved bits—set to default
XTAL_TUNE[7:0]	D7:D0	If Local address 9 D8 = 0, crystal oscillator frequency tuning. 00000000 = Maximum frequency (default) … 11111111 = Minimum frequency If Local address 9 D8 = 1, XTAL DAC current adjustment. xx000000 = 0µA xx000001 = 5µA … xx111111 = 315µA (x = Don't care)

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Table 19. Main Address 30 (A4:A0 = 11110, Main Address 0 D9 = 0)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
LOGEN_BAND[1:0]	D9:D8	LOGEN frequency sub-band for TX spur optimization. 00 = 3.3GHz~3.45GHz 01 = 3.45GHz~3.6GHz (default) 10 = 3.6GHz~3.75GHz 11 = 3.75GHz~3.9GHz
VAS_RELOCK_SEL	D7	VAS relock mode select. This bit is not production tested. For functionality support, contact the manufacturer. 0 = Relock starting at sub-band 15 (default) 1 = Relock starting at present sub-band for short acquisition time
VAS_MODE	D6	VAS operating mode select. 0 = Select VCO sub-band by SPI (VAS_SPI[5:0]) 1 = Select VCO sub-band by VAS (default)
VAS_SPI[5:0]	D5:D0	VAS sub-band SPI overwrite. Active when VAS_MODE = 0. 000000 = Minimum frequency … 011111 = 31 (default) … 111111 = Maximum frequency
VAS_ADC[2:0] (readback only)	D8:D6	Active when VAS_VCO_READOUT (Local address 16 D9) = 1. Read out VAS_ADC[2:0]
VCO_BSW[5:0] (readback only)	D5:D0	Active when VAS_VCO_READOUT (Local address 16 D9) = 1. Read out VAS_BSW[5:0]

Table 20. Local Address 7 (A4:A0 = 00111, Main Address 0 D9 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D5	Reserved bits—set to default
ts_adc[4:0] (readback only)	D4:D0	Temperature sensor's 5-bit ADC output read-out. Activate select by setting Local address 7 D5 = 0.

Table 21. Local Address 9 (A4:A0 = 01001, Main Address 0 D9 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9	Reserved bits—set to default
XTAL_DAC_EN	D8	External VCTCXO tuning DAC. Work with 1% 8.2kΩ resistor at pin XTAL_DAC. 0 = Disable (default) 1 = Enable except during shutdown
CLKOUT_DRV[1:0]	D7:D6	CLKOUT buffer drive. 0 = 1x drive (default) … 3 = 4x drive
RESERVED	D5:D0	Reserved bits—set to default

Table 22. Local Address 14 (A4:A0 = 01110, Main Address 0 D9 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D5	Reserved bits— set to default
PADAC_DIVH	D4	PA DAC clock divide ratio. This bit is not production tested. For functionality support, contact the manufacturer. 0 = For crystal clock at or near 20MHz 1 = For crystal clock at or near 40MHz (default)
PADAC_DLY[3:0]	D3:D0	PADAC turn-on delay control. 0000 = 0µs 0001 = 0µs 0010 = 0.45µs … 0011 = 0.89µs (default) … 1111 = 6.25µs

Table 23. Local Address 15 (A4:A0 = 01111, Main Address 0 D9 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
RESERVED	D9:D5	Reserved bits—set to default
LOGEN_2GM	D4	LOGEN Rx/Tx Gm enable 0 = Depends on Rx/Tx ENABLE pins (default) 1 = Enable both Rx/Tx outputs (required for Rx loopback calibration)
RESERVED	D3:D2	Reserved bits—set to default
REF_DIV[1:0]	D1:D0	Reference divider ratio. 0 = Divide-by-1 (default) 1 = Divide-by-2 2 = Divide-by-4

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Table 24. Local Address 16 (A4:A0 = 10000, Main Address 0 D9 = 1)

BIT NAME	BIT LOCATION (D0 = LSB)	DESCRIPTION
VAS_VCO_READOUT	D9	VAS output read-out from Main address 30. 0 = Read out the SPI register values of Main register 30 (default) 1 = Read out the VAS_ADC[2:0] and VCO_BSW[5:0] bits from the VAS block through Main address 30
DIE_ID_READ	D8	Die type and revision ID read access. 0 = Disable and allow readback of the SPI write values 1 = Read out die type ID from Main address 21 D9:D7 and revision ID from Main address 21 D6:D4 (default)
RESERVED	D7:D0	Reserved bits—set to default

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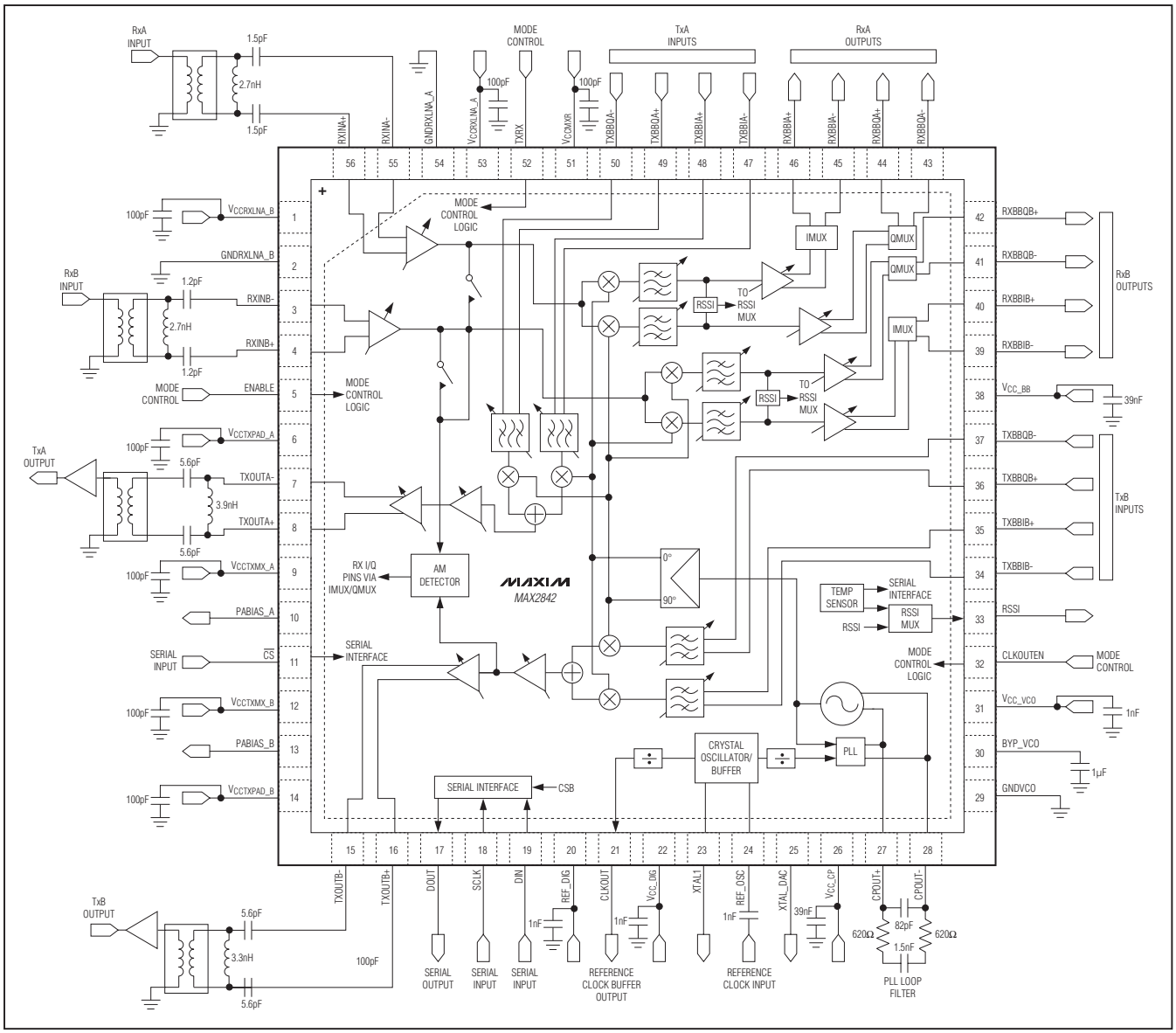
Typical Operating Circuit



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Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
56 TQFN-EP	T5677+2	21-0144	90-0043

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	5/10	Updated Function of XTAL1 in *Pin Description*, added Soldering Temperature to *Absolute Maximum Ratings*	2, 19